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MC68SZ328P/D
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# MC68SZ328

# MC68SZ328 (DragonBall™ Super VZ) Integrated Portable System Processor Product Brief

The DragonBall series of microprocessors is specifically designed for advanced information appliances and messaging applications including PDAs, smart phones, web appliances, and next-generation wireless communicators. To meet these market needs, Motorola continues to build on the popularity of the DragonBall series with the introduction of the DragonBall Super VZ.

The DragonBall Super VZ is the fourth generation in the DragonBall series of products. DragonBall Super VZ is designed to save system and software designers' time by reducing programming steps with increased software re-use, to decrease the overall system cost with additional on-chip peripherals, and to provide an increase in performance.

The major enhancements the new DragonBall Super VZ provides compared to previous versions of DragonBall processors include:

- Improved system speed
- TFT color LCD support
- A/D converter (ADC) with touch panel control
- MMC/SD and Memory Stick™ host controllers
- DMA controller
- Embedded SRAM
- USB device controller
- $I^2C$ interface

All these features combine to make the DragonBall Super VZ the microprocessor of choice among system designers. Its functionality and glue logic are optimally connected, timed with the same clock, fully tested, and uniformly documented. The primary package is a 196-pin MAP BGA designed to occupy the smallest possible footprint on your board.

With several generations of handheld computer processors, the DragonBall series of microprocessors provides designers of handheld portable products with:

- Just the right performance.
- Just the right integration.
- Just the right battery life.

The DragonBall series gives manufacturers and design engineers the ability to create exceptional products that take consumers where they want to go—with mobility, connectivity, scalability, and enhanced freedom.

# 1 Block Diagram

Figure 1 is a simplified functional block diagram of the MC68SZ328.

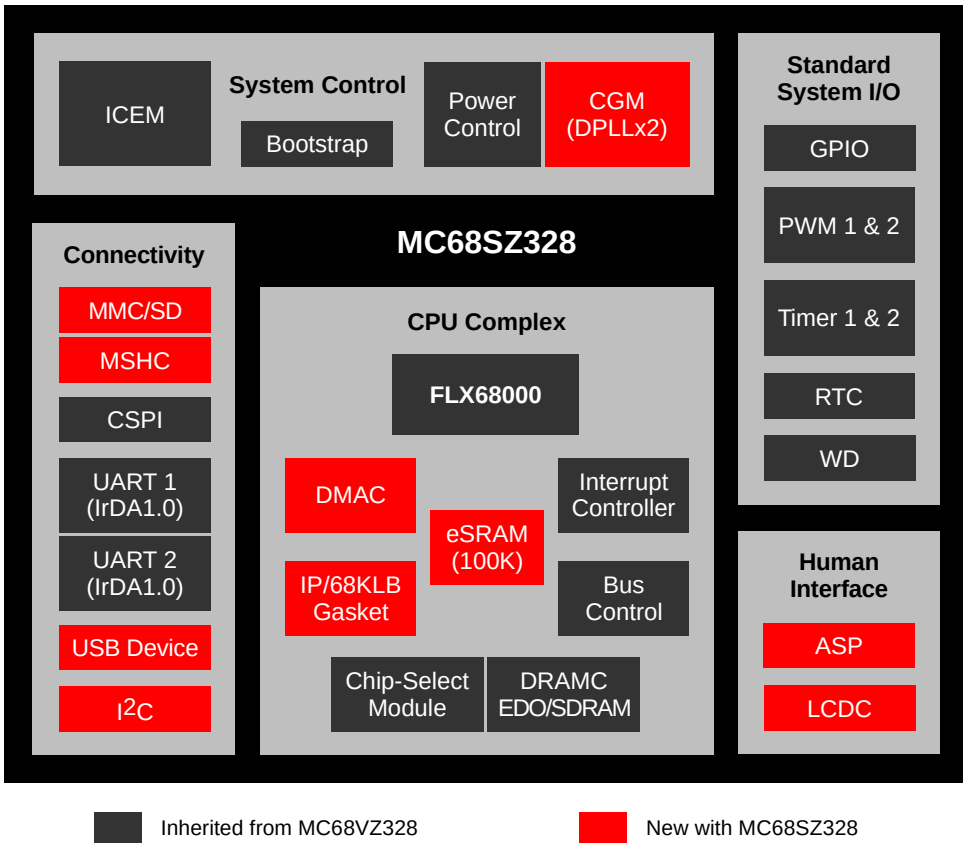


**Figure 1. MC68SZ328 Functional Block Diagram**

# 2 Features

The MC68SZ328 boasts a robust array of features that support a wide variety of applications. The features of the MC68SZ328 include the following:

- Static FLX68000 CPU—identical to MC68EC000 microprocessor
  - Full compatibility with MC68000 and MC68EC000
  - 32-bit internal address bus and 16-bit data bus
  - Static design allows processor clock to be stopped for power saving
  - 66.32 MHz processor clock
  - External M68000 bus interface with selectable bus sizing for 8-bit and 16-bit data ports
- Clock generation module (CGM) and power control module
  - Digital PLLs (phase-locked loops) for all internal clock generation
  - Dual crystal inputs:
    - 32.768 kHz for DMA clock, CPU clock, system clock, LCD clock, and optionally USB clock generation
    - Separate crystal input for USB clock generation
  - Support for three power modes for different power consumption needs: normal, doze, and sleep
  - Programmable processor clock frequency from DC to 66.32 MHz for different bandwidth requirements
- Chip-select module
  - 12 chip-select signals: 10 general-purpose, programmable chip-select signals for external devices with programmable wait state and base address; 1 signal to select eSRAM; 1 signal for the emulation module.
  - Up to 32 Mbyte per chip-select (with a total of 4 Gbyte programmable space for address mapping).
  - Each chip-select can be configured to address an 8-bit or 16-bit space. Both 8-bit and 16-bit contiguous address memory devices can be mixed on a 16-bit data bus system.
  - Glueless interface to SRAM, EDO DRAM, SDRAM, EPROM, and flash memory.
- DRAM controller (DRAMC)
  - Two chip-select signals for supporting either SDRAM or EDO DRAM (self-refresh type only).
  - Each chip-select supports four banks of single data rate 64 Mbit, 128 Mbit, and 256 Mbit SDRAM with up to four banks active simultaneously.
  - Support for 4 Mbit, 16 Mbit, and 64 Mbit self-refresh-type EDO DRAM with 8, 9, 10, and 11 column addresses.
  - Configurable row cycle delay (tRC), row precharge delay (tRP), row-to-column delay (tRCD), and column-to-data delay (CAS latency).
  - Programmable refresh rate.
  - Data retention capability during normal system reset.
  - Support for power-down mode and self-refresh mode for SDRAM power saving.
  - Support for self-refresh mode for EDO DRAM power saving.

- Embedded SRAM (eSRAM)
  - 100K (102,400 bytes) general-purpose internal SRAM
- Direct memory access controller (DMAC)
  - Provides two memory-to-memory channels and four I/O-to-memory or memory-to-I/O channels.
  - Supports 8-bit and 16-bit FIFO and memory port size for data transfer.
  - Supports modules shown in Table 1.
  - Provides data transfer complete and error (burst time-out or request-out) interrupts to interrupt controller. DMA burst length is configurable for each channel.
  - Provides bus utilization control for memory channels.
  - Generates DMA burst time-out error for both memory and I/O channels to terminate DMA cycle when the burst cannot be completed in a programmed timing period.
  - Generates DMA request time-out error for I/O channels to interrupt 68K core when a DMA request is not expected during a programmed timing period.
  - Supports repeat data transfer function.
  - Supports block transfer function to speed up display functions such as image block movement in LCD display, retrieval of pre-store image pattern, and window effect.
  - Provides two external DMA request pins for external devices to initiate data transfer in memory channels 0 and 1, respectively.

**Table 1. Modules with DMA Support**

| Module | DMA Capability |
|---|---|
| CSPI | Yes |
| UART 1 and 2 | Yes |
| USB | Yes |
| MMC/SD | Yes |
| MSHC | Yes |
| ASP | Yes (enhanced ADC) |
| $I^2C$ | No |
| PWM 1 and 2 | No |
| Timer 1 and 2 | No |
| RTC | No |
| Bootstrap | No |

- LCD controller (LCDC)
  - Support for single-screen (non-split), color or monochrome LCD panels and self-refresh-type LCD panels
  - Panel sizes and summary of color and monochrome support are shown in Table 2 on page 5 and Table 3 on page 6

— Support for 4 bpp (bits per pixel) and 8 bpp for passive color panels and support for 4 bpp, 8 bpp, 12 bpp, and 16 bpp for TFT panels
  – Up to 256 colors from a palette of 4096 colors for 8 bpp displays
  – Up to 4096 colors for 12 bpp displays
  – True 64K colors for 16 bpp displays
— 16 simultaneous grayscale levels from a palette of 16 for monochrome displays
— Standard panel interface for common LCD drivers; panel interface of 16-bit, 8-bit, 4-bit, 2-bit, and 1-bit wide LCD panel data bus for monochrome or color panels
— Glueless interface to passive and active color panel (TFT); direct interface to Sharp® 320 × 240 HR-TFT panel
— Use of system memory and embedded SRAM for display memory
— Hardware blinking cursor programmable at a maximum 63 × 63 pixels; support for logical operation between color hardware cursor and background
— Hardware panning (soft horizontal scrolling)
— Hardware assisted landscape and portrait rotation
— Picture enlargement mode that supports pixel doubling function
— 8-bit pulse-width modulator for software contrast control

**Table 2. External Memory Used for Display Memory**

| Panel Type | Bits/ Pixel | Panel Interface (Bits) | Number of Grayscale Levels or Colors | Max. Standard Panel Size Supported (Pixels)[1] |
|---|---|---|---|---|
| Mono-chrome | 1 | 1, 2, 4, 8 | Black and white | 640 x 480 |
| | 2 | 1, 2, 4, 8 | 4 | 640 x 480 |
| | 4 | 1, 2, 4, 8 | 16 | 640 x 480 |
| CSTN | 4, 8 | 8 | 16, 256 | 640 x 480 |
| TFT | 4, 8 | 16 | 16, 256 | 640 x 480 |
| | 12, 16 | 12,16 | 4096, 64K | 640 x 480 |

1. The actual maximum panel size is constrained by system bandwidth use.

**Table 3. eSRAM Used for Display Memory**

| Panel Type | Bits/ Pixel | Panel Interface (Bits) | Number of Grayscale Levels or Colors | Max. Standard Panel Size Supported (Pixels)[1] |
|---|---|---|---|---|
| Mono-chrome | 1 | 1, 2, 4, 8 | Black and white | 640 x 480 |
| | 2 | 1, 2, 4, 8 | 4 | 640 x 480 |
| | 4 | 1, 2, 4, 8 | 16 | 320 x 240 or 240 x 320 |
| CSTN | 4, 8 | 8 | 16, 256 | 320 x 240 or 240 x 320 |
| TFT | 4, 8 | 16 | 16, 256 | 320 x 240 or 240 x 320 |
| | 12, 16 | 12, 16 | 4096, 64K | 240 x 160 or 160 x 240 |

1. The actual maximum panel size is constrained by the size of eSRAM.

- Analog signal processing (ASP) module
  - ADC (16-bit resolution, 12-bit accuracy) with 3 inputs for touch panel and low voltage detect
  - Enhanced ADC (16-bit resolution, 12-bit accuracy) for use as second ADC with DMA support
  - Embedded touch panel circuitry
  - Pen ADC that supports auto data sampling at a configured sample rate
  - Interrupt-based operation with 12 × 16 FIFO for pen ADC sample data and two 8 × 16 FIFOs for data for enhanced ADC
  - Significantly reduced software overhead for pen input applications
  - Low power management
- Timers
  - Two identical 16-bit general-purpose timers/counters
  - Capability to cascade timers together to operate as a single 32-bit timer
  - Input capture capability with programmable trigger edge for interval measurement
  - 15 ns resolution at 66.32 MHz system clock
  - Timer input/output pin for event notification
- Real-time clock and sampling timer (RTC)
  - 32.768 kHz clock input
  - Full clock function: second, minute, hour, and day (up to 512 days)
  - One programmable alarm with interrupt capability
  - Sampling timer with selectable frequency (4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 256 Hz, 512 Hz) and interrupt capability that can be used for digitizer sampling or keyboard debouncing
- Watchdog timer (WD)
  - Programmable watchdog interrupt or reset
- Pulse-width modulation (PWM) modules
  - 8-bit (PWM 1) and 16-bit (PWM 2) resolution
  - 5-byte FIFO in 8-bit PWM 1 provides more flexibility on performance

- Capability to generate high quality sound, tone, or melody

- Interrupt controller
  - All interrupts are maskable.
  - Interrupt level of all internal modules is configurable.
  - Four dedicated external interrupt IRQ signals (defined interrupt level; programmable edge, level, and polarity).
- General-purpose I/O (GPIO) ports
  - 93 total I/O ports in 12 groups with interrupt capability, all multiplexed with peripheral functions.
  - All ports are specially designed with dedicated internal pull-up and pull-down resistors.
- Multimedia card and secure digital (MMC/SD) host controller
  - Compatible with the MMC system specification version 2.2
  - Compatible with the SD Memory Card specification 1.0
  - Ability to achieve maximum data rate with up to 10 cards; only 1 SD card is allowed
  - Password protection of cards
  - Multi-SD function support
  - Error auto-detection for Response CRC and time-out and Access CRC and time-out errors
  - Built-in 7 and 16 CRC generation and checking for command and data
  - Built-in programmable frequency counter for MMC/SD host controller bus
  - Maskable hardware interrupt for internal status and FIFO status indicator
  - 16-bit internal data operation, 8 × 16-bit FIFO, and DMA interface
  - Automatic operation pause when internal FIFO full, allowing flexible packet transaction for dynamic DMA transfer
  - Built-in 3-bit prescaler and 3-bit bus clock divider to maximize the performance of data transaction between memory card and host
- Memory Stick host controller (MSHC)
  - Built-in 8-byte (4-word) FIFO buffer for transmit and receive
  - Built-in CRC circuit
  - Support for internal or external serial clock source
  - Built-in Serial Clock Divider: maximum 33.16 MHz serial data transfer rate
  - DMA supported; DMA request condition is selectable based upon FIFO status
  - Automatic command execution when an interrupt from the Memory Stick is detected (can be turned on/off)
  - RDY time-out period can be set by the number of serial clock cycles
  - Interrupt can also be output to the core when a time out occurs
  - Two built-in general-purpose input pins for detecting Memory Stick insertion/extraction
  - 16-bit host bus access (byte access not supported)

- Universal asynchronous receiver/transmitters (UARTs)
  - Two identical UARTs with interrupt-based operation
  - Support for serial data transmit/receive operation: 7 or 8 data bits, 1 or 2 stop bits, programmable parity (even, odd, or none)
  - Programmable standard baud rates up to 460.8 kbps
  - Receive FIFO size is 32 bytes; transmit FIFO size is 32 bytes
  - Both UARTs IrDA 1.0 ready
  - Maximum non-standard baud rate of 4.14 Mbps
  - Flexible DMA burst access to both UART 1 and UART 2 FIFO architectures
- Configurable serial peripheral interface (CSPI)
  - Master/slave configurable
  - 8 × 16 data-in FIFO and 8 × 16 data-out FIFO
  - Flow control signals incorporated to enable fast data communication
- Reset module
  - Provides stable system power-on reset and normal reset
- Bootstrap mode function
  - Allows user to initialize system and download programs or data to system memory through either UART
  - Accepts execution command to run program stored in system memory
  - Provides a 32-byte-long instruction buffer for 68000 instruction storage and execution
- Universal Serial Bus (USB) device
  - Compliant with Universal Serial Bus Specification revision 1.1.
  - Endpoint configurations are as shown in Table 4 on page 9. Five pipes are available for mapping.
    - Endpoint 0 is required by the USB specification.
    - Endpoints 1, 2, 3, and 4 may be configured as bulk or interrupt pipes (IN or OUT).
  - A frame match interrupt feature is supported to notify the user when a specific USB frame occurs. For DMA access, the maximum packet size for each endpoint is restricted by the FIFO size of the endpoint.
  - Four bulk/interrupt pipes are supported for 12 Mbps data transfer. The packet sizes are limited to 8, 16, 32, or 64 bytes, and the maximum packet size depends on the FIFO size of endpoint.
  - No power drawn from the USB bus.
  - Remote wake-up feature is supported via a register bit.
  - Complete FIFO interrupts are provided (full, empty, error, high, low).
  - End-of-frame and start-of-frame interrupt support.
  - Full-speed (12 MHz) operation.
  - Intelligence related to packet retries and data framing is built into the FIFO controller.

**Table 4. Endpoint Configurations**

| Endpoint | Direction | Physical FIFO Size (Bytes) | Endpoint Configuration | Maximum Packet Size |
|---|---|---|---|---|
| 0 | IN and OUT | 32 | Control | 16 |
| 1 | IN or OUT | 16 | Bulk or interrupt | 16 |
| 2 | IN or OUT | 16 | Bulk or interrupt | 16 |
| 3 | IN or OUT | 128 | Bulk or interrupt | 64 |
| 4 | IN or OUT | 128 | Bulk or interrupt | 64 |

- Inter-IC ($I^2C$) bus module
  - Compliant with Philips $I^2C$-bus standard (support for Standard-mode and Fast-mode)
  - Support for 7-bit address
  - Support for 3.0 V devices
  - Multiple-master operation
  - Software-programmable for 1 of 64 different serial clock frequencies
  - Software-selectable acknowledge bit
  - Interrupt-driven, byte-by-byte data transfer
  - Arbitration-lost interrupt with automatic mode switching from master to slave
  - Calling address identification interrupt
  - Start and stop signal generation and detection
  - Repeated START signal generation
  - Acknowledge bit generation and detection
  - Bus-busy detection
- In-circuit emulation module (ICEM)
  - Dedicated memory space for emulator debug monitor with chip-select
  - Dedicated interrupt (interrupt level 7) for in-circuit emulation
  - One address-signal comparator and one control-signal comparator, with masking to support single or multiple hardware execution breakpoints
  - One breakpoint instruction insertion unit
- Operating system frequency
  - Up to 66.32 MHz
- Operating voltages
  - Core operates at 1.8 V
  - Supply voltage: 2.7 V to 3.3 V
- Package type
  - 196-pin MAP BGA
  - Size: 12 mm × 12 mm
  - Pitch size: 0.8 mm

# 3 DragonBall Series Comparison

The DragonBall Super VZ marks the fourth generation in the DragonBall series. Table 5 compares the new processor with previous generations. The shaded cells indicate the features that are available for the first time on the MC68SZ328.

**Table 5. DragonBall Series Comparison**

| Feature | DragonBall | DragonBall EZ | DragonBall VZ | DragonBall Super VZ |
|---|---|---|---|---|
| **CPU** | 68EC000 | 68EC000 | FLX68000 | FLX68000 |
| **LCD controller** | Up to 4 gray (1024 x 512) | Up to 16 gray (320 x 240), 2 gray (640 x 512) | Up to 16 gray (640 x 512) | Up to 16 gray for monochrome Up to 256 colors for passive Up to 64K (16-bit) colors for active TFT |
| **Chip-selects** | 16 | 8 (external), 1 (EMUCS) | 8 (external), 1 (EMUCS) | 10 (external), 1 ($\overline{\text{EMUCS}}$), 1 (internal SRAM) |
| **DRAM controller** | Not provided | Provided | Provided (supports EDO DRAM and SDRAM) | Provided (supports EDO DRAM and SDRAM) |
| **PLL and power control** | Provided | Provided | Provided | Provided (digital PLL) |
| **Interrupt controller** | Provided | Provided | Provided | Provided |
| **Timers** | 2 | 1 | 2 | 2 |
| **RTC** | 1 | Enhanced (with sampling timer) | Enhanced (with sampling timer) | Enhanced (with sampling timer) |
| **SPI 1** | Master (SPIM) | Master | Master/slave | Master/slave |
| **SPI 2** | Slave (SPIS) | Not provided | Master | Not provided |
| **UART (with infrared interface)** | 1 | 1 | 2 | 2 |
| **16-bit PWM** | Provided | Not provided | Provided | Provided |
| **8-bit PWM** | Not provided | Provided | Provided | Provided |
| **ICEM** | Not provided | Provided | Provided | Provided |
| **Bootstrap** | Not provided | Provided | Provided | Provided |
| **GPIO** | 77 | 54 | 76 | 93 |
| **ASP** | Not provided | Not provided | Not provided | Provided (with touch panel control circuitry) |
| **MMC/SD host controller** | Not provided | Not provided | Not provided | Provided |
| **Memory Stick host controller** | Not provided | Not provided | Not provided | Provided |
| **DMA** | Not provided | Not provided | Not provided | Provided |

**Table 5. DragonBall Series Comparison (Continued)**

| Feature | DragonBall | DragonBall EZ | DragonBall VZ | DragonBall Super VZ |
|---|---|---|---|---|
| **Embedded SRAM** | Not provided | Not provided | Not provided | 100 Kbyte |
| **USB Device** | Not provided | Not provided | Not provided | Provided |
| **$I^2C$** | Not provided | Not provided | Not provided | Provided |
| **Speed** | Up to 16.58 MHz | Up to 16.58 MHz and 20 MHz | Up to 33.16 MHz | Up to 66.32 MHz |
| **Voltage** | 3.0 V to 3.6 V<br>4.5 V to 5.5 V | 3.0 V to 3.6 V | 2.7 V to 3.3 V | 2.7 V to 3.3 V |
| **Packages** | 144-pin TQFP | 100-pin TQFP, 144-pin BGA | 144-pin TQFP, 144-pin MAP BGA | 196-pin MAP BGA |

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