10.2.3 Summary of Port Behavior During Reset

Table 10-2 summarizes the behavior of all MC68VZ328 I/O ports during the Reset Assertion Time Length (see Figure 10-1 on page 10-3) for power-up resets and warm resets.

Table 10-2. MC68VZ328 I/O Port Status During the Reset Assertion Time Length

I/O Ports	Warm Reset	Power-up Reset
A	Resets to default state	Resets to default state
B	Maintains previous state	Unknown state
C	Resets to default state	Resets to default state
D	Resets to default state	Resets to default state
E	Resets to default state	Resets to default state
F	Resets to default state	Resets to default state
G	Resets to default state	Resets to default state
J	Resets to default state	Resets to default state
K	Resets to default state	Resets to default state
M	Maintains previous state	Unknown state

Note: The default state is defined by the reset values of the corresponding I/O port's registers. Please refer to Table 3-1 on page 3-2 and Table 3-2 on page 3-8 for details.

10.3 I/O Port Operation

The following subsections describe details of the I/O ports' operation.

10.3.1 Data Flow from the I/O Module

The operation of a port connected to another module in the MC68VZ328 is illustrated in Figure 10-2 on page 10-5.

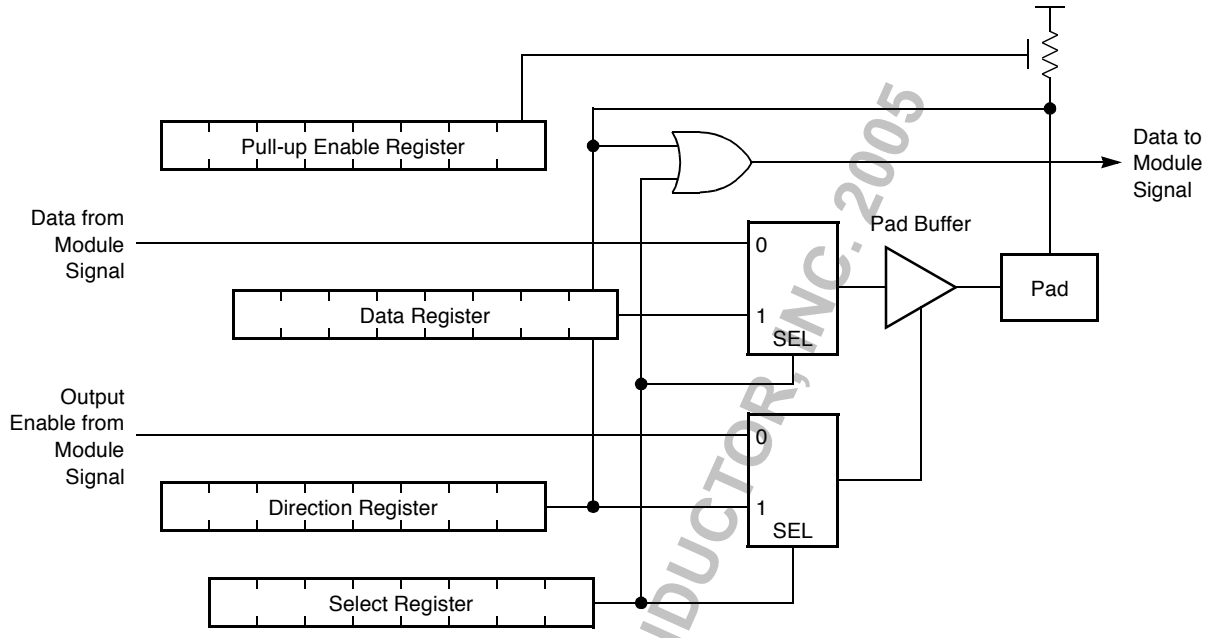

Figure 10-2. I/O Port Operation

For example, if Figure 10-2 represents the D0 bit of Port E, when the SEL0 in the select register is cleared, the "data from module" line is connected to the serial peripheral interface module's TXD signal (SPITXD). Because SPITXD is output-only, the MC68VZ328 asserts the "output enable from module" line, thus enabling the output and disabling the "data to module" line. As long as the SELx bit of the port's select register is clear (the default is set at reset), the SPI module pin function is enabled. Bit D0 of Port E is the master SPMTXD signal. The SPI module controls the direction of data flow for the pin, which is always output. When the dedicated module controls the port, the direction register is ignored. There are a few exceptions that are described in the individual port programming sections that follow.

10.3.2 Data Flow to the I/O Module

An example of data flow to the I/O module is the D1 bit of Port E. This signal's function is the SPI's RXD (SPIRXD) signal. In this case, SPIRXD is input-only; thus, the chip negates the "output enable from module" line, and the "data from module" line is not disabled (see Figure 10-2). The "data to module" signal is connected to the SPIRXD input of the SPI.

10.3.3 Operating a Port as GPIO

While the SELx bit is set (if the DIRx bit of the PxDIR is 1), data written to the port's data register is presented to the pin. If the DIRx bit in the direction register is 0 (input), data present on the pin is sampled and presented to the CPU when a read cycle is executed. While the DIRx bit is 0 (output), the actual pin level is presented during write accesses. This may not be the same as the data that was written if the pin is overdriven. To prevent data loss when changing from one mode to another, the intended data should be written to the PxDATA register before entering the selected mode.